AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (currently amended) A nonvolatile memory comprising:

a memory array unit having a plurality of nonvolatile memory cells;

a control unit; and

a voltage generating unit for supplying voltages to said nonvolatile memory cells,

wherein said nonvolatile memory cells store information corresponding to ~~the~~ a quantity of electric charges in a floating gate of each nonvolatile memory cell,

wherein said control unit controls a write operation to store information into said nonvolatile memory cells~~,~~, a read operation to read information stored in said nonvolatile memory cells; and an erase operation to erase information stored in said nonvolatile memory cells,

wherein said voltage generating unit has an erase voltage generating unit for generating, in accordance with control from said control unit, erase voltages to be applied to said nonvolatile memory cells in said erase operation, and

wherein said erase voltage generating unit generates, ~~on the basis of~~ in response to a control signal supplied from said control unit, erase voltages of two or more levels including a lower erase voltage and a higher erase voltage, and

wherein said control unit performs control such that in said erase operation the lower erase voltage is applied ~~applying them~~ to a control gate of each of said nonvolatile memory cells and thereafter the higher erase voltage is applied to the control gate of each of said nonvolatile memory cells.

2. (currently amended) A nonvolatile memory comprising:

a memory array unit having a plurality of nonvolatile memory cells;

a control unit; and

a voltage generating unit for supplying voltages to said nonvolatile memory cells,

wherein said nonvolatile memory cells store information corresponding to ~~the~~ a quantity of electric charges in a floating gate of each nonvolatile memory cell,

wherein said control unit controls a write operation to store information into said nonvolatile memory cells~~,~~, a read operation to read information stored in said

nonvolatile memory cells; and an erase operation to erase information stored in said nonvolatile memory cells,

wherein said voltage generating unit has an erase voltage generating unit for generating, in accordance with control from said control unit, erase voltages to be applied to said nonvolatile memory cells in said erase operation, and

wherein said erase voltage generating unit generates, ~~on the basis of~~ in response to a control signal supplied from said control unit, erase voltages of two or more levels to make ~~the~~ voltages applied to ~~the~~ tunnel films of said nonvolatile memory cells substantially constant and applies ~~them~~ the erase voltages selectively to a control gate of each of said nonvolatile memory cells.

3. (currently amended) The nonvolatile memory according to Claim 2, wherein said control unit performs control to verify ~~erase voltage generating unit, after applying erase voltages of two or more different levels to said control gates of~~ whether information stored in said nonvolatile memory cells~~, verifies the erase~~ is erased after a plurality of the erase voltages have been applied to the control gate of each of said nonvolatile memory cells.

4. (original) The nonvolatile memory according to Claim 3, wherein, out of the erase voltages generated by said erase voltage generating unit, a first voltage level of an erase voltage first applied to said control gate of any of said nonvolatile memory cell is the lowest, and each of the erase voltages applied second and afterwards is higher in level than the erase voltage applied immediately before.

5. (cancelled).

6. (cancelled).

7. (cancelled).

8. (currently amended) A nonvolatile memory comprising, on one semiconductor substrate~~,~~:

a memory array unit;

a control unit; and

a voltage generating unit,

wherein said memory array unit has a plurality of word lines and a plurality of nonvolatile memory cells,

wherein each ~~of the~~ said nonvolatile memory cells ~~has~~ includes a first terminal connected to a first semiconductor region~~,~~, a second terminal connected to a second

semiconductor region~~,~~ and a third terminal connected to a control gate~~,~~

wherein ~~there~~ a channel region is disposed between said first semiconductor region and said second semiconductor region, an electric charge accumulating region ~~above a channel region~~ is disposed between the control gate and the channel region, ~~between said first semiconductor region and said second semiconductor region and between it and said control gate;~~ and ~~there is~~ a first insulating film is disposed between the electric charge accumulating region and the channel region,

wherein the third terminal of at least one said nonvolatile memory cell is connected to each word line,

wherein data are stored into each nonvolatile memory cell according to ~~the~~ a quantity of electric charges accumulated in said electric charge accumulating region; and the quantity of electric charges is controlled by ~~the control of~~ said control unit ~~over~~ performing a first operation to inject electric charges into said electric charge accumulating region and a second operation to eject electric charges ~~out of~~ from said electric charge accumulating region,

wherein, in order to perform said second operation, a first voltage generated by said voltage generating unit is

applied between said control gate and said channel region via a word line connected to the control gate, and

wherein, during ~~the~~ a period of said second operation, ~~the~~ said first voltage generated by said voltage generating unit is varied ~~twice~~ two or more times, so as to keep ~~the~~ voltage applied to said first insulating film within a ~~predetermined~~ first voltage range.

9. (currently amended) The nonvolatile memory according to Claim 8,

wherein, during said first operation, ~~the~~ a second voltage generated by said voltage generating unit is applied between said control gate and said channel region via ~~a~~ the word line connected to the control gate, and

wherein, during said first operation, ~~the~~ said second voltage generated by said voltage generating unit is varied.

10. (currently amended) The nonvolatile memory according to Claim 9, wherein~~, the~~ said first voltage applied between said control gate and said channel region in said first operation differs in polarity from ~~the~~ said second voltage applied between said control gate and said channel region in said second operation.

11. (currently amended) The nonvolatile memory according to Claim 10,

wherein the threshold voltage of ~~the~~ each nonvolatile memory cell~~s~~ is varied according to the quantity of electric charges accumulated in said electric charge accumulating region so as to be included in a plurality of threshold voltage distributions according to data to be stored into said nonvolatile memory cell~~s~~,

wherein in said first operation, the threshold voltage of ~~the~~ at least one said nonvolatile memory cell~~s are~~ connected to one word line is moved into a first threshold voltage distribution, and a first determination is made during said first operation as to whether ~~or not~~ the threshold voltage of ~~the~~ said at least one nonvolatile memory cell~~s are~~ is moved within said first threshold voltage distribution, and

wherein in said second operation, the threshold voltage~~s~~ of all of the nonvolatile memory cells connected to said one word line are moved into a second threshold voltage distribution~~,~~ and a second determination is made during said second operation as to whether ~~or not~~ the threshold voltage~~s~~ of ~~the~~those nonvolatile memory cells are moved within said second threshold voltage distribution[[,]]

~~wherein said threshold voltage of at least one of a plurality of nonvolatile memory cells connected to one word line is moved, in said first operation, and~~

~~wherein said threshold voltages of all of the plural nonvolatile memory cells connected to one word line are moved, in said second operation~~.

12. (new) The nonvolatile memory according to Claim 1, wherein said control unit performs control to verify whether information stored in said nonvolatile memory cells is erased after said higher erase voltage has been applied to the control gates of said nonvolatile memory cells.

13. (new) The nonvolatile memory according to Claim 12, wherein the level of said lower erase voltage is lower than the levels of other erase voltages generated by said voltage generating unit.